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Directory: /class2/ug24/a240152x/EE3408C\_pdk180nm/Assignment/ Sub#2dProject\_1

# Introduction (background and objectives)

This project is focused on designing a sing-stage Common Source amplifier with CSL. This amplifier must follow the specifications detailed below.

* Supply voltage (VDD)of 1.8 V
* Open-loop DC Gain: > 40dB
* Output voltage swing: > 1.0 Vp-p
* DC output voltage: ~ 0.9 V
* Total current: < 0.4 mA
* Maximum channel width: 500 μm

The circuit layout is detailed below:

A diagram of a circuit

Description automatically generated

Figure 1. Template circuit provided

It is understood that the amplification is performed by M1. M2, along with the mirror current, helps to set the drain current which flows through M1. With this understanding, the two halves of the circuit is considered separately.

# Circuit design with necessary hand calculations

First, both M1 and M2 MOSFETS must operate in saturation mode to operate as an amplifier.

Given the specifications, Voutput is expected to swing between 0.4V to 1.4V at least. Hence, the maximum overdrive voltage for M1 and M2 to be 0.4V. We will assume 0.2V as the overdrive voltage.

Along with the value of VOD, we also assume the DC component of Voutput is 0.9V, and the drain current of M1 and M2 is 25μA.

For M1,

VOD > VSG – |VTHP|

VSG < 0.2 + 0.45

VSG < 0.65V

1.8 - VG < 0.65V

VG > 1.15V

Similarly, for M2,

VOD > VGS – VTHN

VGS < 0.2 + 0.32

VGS < 0.52V

VG - 0 < 0.52V

VG < 0.52V

Hence, 1.2V and 0.5V are applied to the gates of M1 and M2 respectively to bias both MOSFETs to operate in saturation mode.

Next, we calculate the ratio of the sizing of M2 MOSFET. This is calculated using the drain current equation.

ID = 0.5 \* kn \* (W/L)n \* (VGS - VTHN)2 \* (1 + λ \* VDS)

With kn = 4.9 \* 10-5, ID = 25μA, VGS = 0.6V

(W/L)n = 30.399… = 30.4 (3 s.f)

The sizing ratio of M1 MOSFET is calculated using the gm equations.

VOD = 2\*ID / gm

gm = 2\*ID / VOD

gm = (2 \* 25\* 10-6) / (0.6 – 0.45) = 2x10-4

Using relationship gm = 2 \* ID / VOD

gm = 2 \* ID / VOD = 2 \* (0.5 \* kp \* (W/L)p \* VOD2) / VOD= kp \* (W/L)p \* VOD

(W/L)p = 2\*10^-4 / (3.6\*10-5) / (0.5 - 0.32)

= 30.864… = 30.9 (3 s.f.)

After obtaining these ratios, arbitrary values of width and length of the MOSFETs are calculated, starting from length L of 1u for both. The amplifier is first constructed in Cadence Spectre software without the current mirror components. The calculated sizing of the MOSFETs were inputted and tuned one variable at a time to obtain a DC output voltage of round 0.9V, and a peak-to-peak voltage of more than 1V.

A computer screen shot of a computer program

Description automatically generated

Figure 2. Amplifier circuit was constructed first, and fine-tuned later

After finetuning the MOSFETS, the actual drain current of M1 and M2 were noted down to calculate for the resistance on the current mirror side of the circuit.

From the simulation, the actual drain current is 32.4668uA, slightly higher than that assumed. Since M2 and M3 forms a current mirror, we take M2 and M3 to have the same sizing.

RB1 = (1.8 - 0.5) / (32.4668 \* 10-6) = 40040.90…Ω

After this, the full circuit is constructed, and further fine-tuning is conducted to meet the requirements.

# Cadence Spectre simulation results

A computer screen shot of a computer program

Description automatically generated

Figure 3. Final circuit with component parameters.

A computer screen shot of a computer program

Description automatically generated

Figure 4. Final circuit with DC operating point

The transient behaviour is observed when an AC signal with amplitude 0.5mV and frequency of 100kHz is provided.

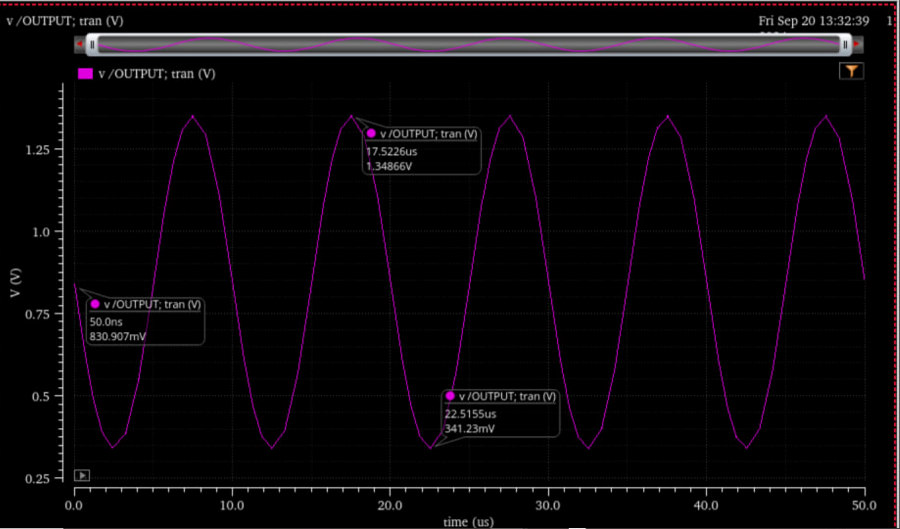


Figure 5. Plot of Voutput

# Observations

From tuning the amplifier, a series of observations can be made. Generally, increasing the width of M1 may increase or decrease the gain of the amplifier at times. This is because the transconductance of M1 is directly proportional to gm, which in turn is directly proportional to Av through Av = gm \* rout. However, increasing the width of M1 also decreases the output resistance of M1, which reduced Av too. The overall increase or decrease in gain is dependent on the other parameters.

Similarly, if the length of M1 is increased, the DC component of Voutput decreases, while increasing the length of M2 will increase the DC component of Voutput. This is because the output resistance of the transistors is directly proportional to its length, which results in greater voltage drop across the VDS of the transistor whenever its length is increased.

Increasing the width of M2 decreases drain current of M1, hence resulting in a smaller voltage drop across VDS of M2, leading to decreasing DC component of Voutput.

# Discussions of results and observations

From Figure 5, the output swings from 0.34123V to 1.34866V, providing a peak-to-peak voltage swing of 1.00743V. Since the input AC signal has an amplitude of 5mV,

Gain = 20 \* lg(1.00743 – (5 \* 10-3 \* 2)) = 40.064… = 40.0dB (3 s.f)

The DC component of the Voutput is 0.840746V, very close to the required 0.9V.

The current drain of M3 is 32.4476μA and that of both M1 and M2 is 33.0894μA.

Total current flow = 32.4476 + 33.0894 = 65.537μA < 0.4mA

The maximum channel width of the MOSFETs did not exceed the 500μm limit.

# Conclusion

In this project, a Common Source amplifier with current source load has been successfully designed to meet the required specifications. The key results of the design include:

* Gain of slightly larger than 40dB
* DC output voltage of 0.840746V
* Peak-to-peak voltage swing of 1.00743V

The circuit was split into two parts for consideration, on the right consisting of the amplifier circuit, and the current mirror on the left. Considering the amplifier circuit first, hand calculations provided rough values to simulate the amplifier’s performance. Further tweaking is required due to unaccounted issues during calculations.

After the first iteration of tweaking, the DC operating point and the resultant drain current through M1 and M2 were noted. From this data, the resistance of the resistor on the current mirror is then calculated, and the rest of the circuit is built and simulated. A second round of tuning is required to ensure that the specifications are met.

Through this project, a better understanding of the relationships of the parameter is appreciated. The workflow on tackling such design problems is also better understood overt the course of the project.